K.V.G. COLLEGE OF ENGINEERING

Kurunjibhag, Sullia, D.K.-574 327, Karnataka, INDIA

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Department of Electronics and Communication Engineering

FACULTY PROFILE

Name of the Faculty	**Dr. SAVITHA. M**
Designation	**Professor**
Contact Numbers	**Office: 08257- 231141** **Mobile: +91 - 9449332086**
E-mail ID	**savith73@gmail.com**

• Educational Qualification

Degree	Specialization	Year of Passing	College & University
B.E	Electrical and Electronics	1995	KVG college of engineering Sullia-Mangalore
M. Tech	Industrial Electronics	2003	NITK Surathkal, NITK
Ph.D.	Mixed Mode VLSI	2020	REVA University Bangalore

• Work Experience

Teaching	Research	Industry
24+Experience	**7+Experience**	**2 year**

• Date of Joining to the College

10th May 1999

• In-House Experience

Designation	Duration		Department
	From	To	
Lecturer	10-05-1999	31-03-2005	E & C
Asst. Professor	01-04-2005	26-02-2012	E & C
Associate Professor	27-02-2012 to 2021		E & C
Professor	2021 to Till the Date		E & C

• Outside Experience

Designation	Place	Duration	
		From	To
Engineer –Trainee	Power Gear Limited, Bangalore	01-08-1996	30-01-1998

• Area of Interest

Analog and Mixed Mode VLSI	Verilog and VHDL Languages	Digital Signal Processing	Power Electronics	CMOS VLSI	Analog and digital circuits

• Subject Taught

For UG:

1. Analog Electronics Circuit
2. Signal and System
3. VLSI Design
4. CMOS VLSI Design
5. Low Power VLSI
6. Digital Signal Processing
7. Analog and mixed Mode VLSI
8. Basic VLSI
9. Power electronics
10. Fundamental of HDL
11. Microelectronics
12. Digital Design using VHDL
13. Embedded system
14. Computer Organization
15. Basic Electronics
16. Verilog HDL
17. Digital system design with Verilog
18. Scientific Foundation of Health
19. Universal Human values

For PG:

1. CMOS VLSI design
2. Research Methodology and IPR
3. Cryptography and network security
4. Advances VLSI Design
5. VLSI design verification
6. Design of CMOS RF circuit
7. Advanced Analog and mixed Mode VLSI
8. Research Methodology

• Membership in Professional Bodies/University Bodies/Organizations

– **Member of Indian Society for Technical Education (MISTE):** LM-37012 (2001)

• Publications

National / International Journals	National / International Conferences
06	05

• Publications : International Journals

1. Shalini M.C, Savitha, M, "*Detection banana grading stages using image processing and machine learning",* International Journal of innovative Research in technology, ISSN 2349-6002
2. Dr. Savitha M, Dr. Bhagya H K, Dr. Kusumadhara S, Adarsha D and Prathima M, "*Implementation of heart rate and temperature monitoring device using wireless system*", International Journal of Creative Research Thoughts, vol 11, issue 7, July 2023
3. Dr. Savitha M ,Dr. Bhagya H K, Dr. Kusumadhara S, and sahana S M ," *Skin Cancer detection using Machine learning and Image Processing* " International Journal of Creative Research Thoughts, vol 11, issue 7, July 2023.
4. Savitha .M, R.Venkat Siva Reddy, "*Dual Split-Three Segment Capacitor Array Design Based Successive Approximation ADC for Io-T Ecosystevm" Integration*", The VLSI Journal https://doi.org/10.1016/j.vlsi.2019.05.004
5. Savitha .M, Venkat Siva Reddy, "*A 14-bit Dual-Split Capacitor Array DAC Design Based Successive Approximation ADC" International* Journal of Recent Technology and Engineering (IJRTE)' at Volume-8 Issue-1, May 2019.
6. Raghavendra, Savitha .M, "*Multi-serial to Ethernet gateway by using FPGA*" International Journal of Recent Technology and Engineering (IJRTE)' at – issue no. 2250-3536, 2012.

• Publications : National / International Conferences

- "14 -bit Low Power Successive Approximation ADC using Two Step Split Capacitive array DAC with multiplexer switching". *IEEE, second ICAECC-2018*
- "FPGA implementation of Fingerprint Verification Based on Fusion of minutiae and Ridges" was presented in *"International Conference on Current Trends in Engineering and Management – ICCTE-M2012"* held on12, 13 &14th July 2012 at Vidyavardhaka College of Engineering, Mysore.
- "Multi-serial to Ethernet gateway by Using FPGA" was presented in "*National conference on Emerging Trends in Technology –NCET-Tech 2O12*" held on 26th - 27th April 2012 at Nagarjuna college of Engineering and Technology, Bangalore.
- "FPGA implementation of realization of efficient BCD adder using reversible logic" was presented in *National Conference on "Advances in Computer Applications-NCACA-2O12* which was held at Sri Siddhartha Institute of Technology, Tumkur, Karnataka on 10th and 11th May 2012.
- "Design and analysis of an efficient double tail comparator using 0.18µm technology" was presented in *National Conference on "Recent trends in Electronics and communication engineering -NCRTEC-14* which was held at SJB institute of technology Bangalore on 10th th May 2014.

• Professional Activities: NPTEL Course

NPTEL (National Program on Technology Enhanced Learning)	Subject	Year of Certification	Result
	1. Teaching and Learning in Engineering (TALE) (Prof. N J Rao, IISc, Bangalore)	March-2019 (4weeks. FDP)	72% (Silver Medal)

• Faculty Development Programmes (FDP) Participated

SL. No.	Program Title	Venue	Date & Year
1.	DSP and its application	SJCE Mysore	25th to 28th March 2008
2.	Faculty training program on internal audit	Power Gear ltd	11th to 12th July 2003
3.	Faculty training program on VLSI design	RNSIT Bangalore	4th to 6th August 2005
4.	Eighth state level convention on ISTE	KVGCE Sullia	18th 19th November
5.	Applications of Artificial intelligence an machine learning	Reva University Bangalore	10th to 14th of May 2021
6	An Overview of Teaching Techniques in Innovation & Design Thinking	VTU Human Resource Development Centre	6th to 10th December 2021
7	"An Overview of Teaching Techniques in Scientific Foundations of Health	VTU Human Resource Development Centre	20th & 24th December 2021
8	"Python –A practical Approach"	KVGCE	13th & 14 of June 2023
9	"Ability Enhancement Courses in Electronics And Communication Engineering "	KVGCE	27th to 29th October 2022
10.	Ability Enhancement Course in Basics of C++	KVGCE	27-07-2023 to 29-07-2023

• Workshops / Short-term Course Attended

SL. No.	Workshop Title	Place	Date & Year
1.	Research Methodology and Latex Documentation	REVA university Bangalore	9th and 10th Jan 2017
2.	Machine dynamics and instrumentation" [MDI _2012]	KVGCE SULLIA	**26th – 30th** March 2012

3.	Mission 10X'	KVGCE SULLIA	20th to 24th December 2010
4.	Faculty training program in power Electronics (theory and lab)	NMAMIT, Nitte	23rd to 28th February 2004
5.	Application on Signal Processing (AICTE sponsored)	SJCE Mysore	2004
6	ASIC Design flow using Mentor graphics tools	CoreEL Technology Bangalore	06th September 2021
7	Designing with CANVA	KVGCE	8th July 2023

• No. of Project Guided

UG	PG
17	**15**

• Responsibilities Taken in College Level

Event	Positions	Duration	
		From	To
PG studies	Director of PG studies	06-06-2022	Till the date
Alumni Association Sullia chapter	Treasurer	2010	Till the date
Language Lab Coordinator	Coordinator	2021	Till the date

• Responsibilities Taken in Department Level

Event	Role	Duration	
		From	To
1. Research and MOU	Coordinator	2021	Till the Date
2. ENCEA	Treasurer	2008	Till the Date
3. VLSI Lab	In- charge	2010	Till the date
4 NBA/NAAC	Coordinator	2012	Till the date
5.Department PAC	Member-Secretary	2021	Till the date

- **Participation details in the college level event.**

SL .No.	Event	Position / Role
1.	College sports meet	Member
2.	Alumni meet	Member and Treasurer
3.	College Day function	Member
4.	Thanthrajna -2017	Member
5	PG- Student welcome program	Chairman

- **Participation details in the Department level activities**

SL .No.	Event	Role / Responsibilities
1.	e-congregation-2004	Chairman -Technical presentation
2	ENCEA activities	Judge for mini project and cultural activities
3.	LAB setup	In -charge for HDL lab, VLSI Lab
4.	Mentoring	Counselor for EC Students & Other dept. activities

- **No. of Lab Manual / Program Guidelines Prepared**

SL. No.	Lab manual / Guide lines Title	Semester and branch	Year
1.	VLSI Lab manual	7th sem E & C	2008 to 2019
2.	VHDL/Verilog Lab manual	4th sem E & C	2008,2017,2021
3	Analog Circuits Lab Manual	4th sem	2021
4	Digital System Design with Verilog Manual	3rd sem	2022

- **No. of Labs handled for UG and PG**

SL. No.	Lab Title	Year	Semester & Branch
1.	Power Electronics Lab	2004	VII E&C
2.	VLSI Lab	2008 to 2021	VII E&C
3.	AEC Lab	2010 to 2021	III E&C

4.	HDL Lab	2004to 2021	IV E&C
5.	Microprocessor Lab	2016, 2017	1V E&C
6.	Embedded Lab	2019	VI E&C

• Interaction with Outside World / Invited Lectures

Sl.No.	Program	Venue and Organizer	Date
1.	Sristi Project Exhibition	Sahyadri College of Engineering	12th to 16th May -2012

• Awards / Recognition / Achievements/ Others

- **Valuator** of VTU Digital Valuation Centre, KVGCE, Sullia for the digital Valuation work of UG/PG answer scripts VTU Examination.
- Served/Serving as **Question Paper setter and Moderator** for UG and PG program for VTU and other reputed autonomous institutes and Universities like NMAMIT @ Nitte, MIT@ Manipal.

Dr. SAVITHA.M, PROFESSOR, E &C DEPT., KVGCE, SULLIA, D.K - 574 327

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